REMARKS

Claims 1-35 are pending and stand rejected in the present application. Claims 1, 12, 19, 27, and 34 have been amended by way of this amendment. Claims 1-35 remain pending and at issue.

Claims 1, 2, 12-14, 19, 20, 25-28, and 34 stand rejected under 35 USC 102(b) as being unpatentable over Brown et al. (U.S. Patent No. 6,360,340).

Amended independent claim 1 and claims 2, 25, and 26 dependent thereon, recite a magnetic memory including *inter alia* at least two magnetic memory cells and a control system, where the at least two magnetic memory cells and the control system are components of the magnetic memory. The at least two magnetic memory cells are configured to store data. The control system is configured to at least twice obtain parametric values from the magnetic memory cells and generate a corresponding compressed fault map using the parametric values. At least one of the compressed fault maps is compared to a previous one of the compressed fault maps and an indication is provided if there are differences.

Brown et al. generally discloses a memory tester for testing semiconductor memory devices. The memory device to be tested is electrically coupled to the memory tester during the testing process and decoupled and removed from the memory tester once testing is complete. In one disclosed embodiment, each memory device is tested under two different testing conditions and the first set of test data generated under the first set of testing conditions is compared with the second set of test data generated under the second set of testing conditions. The generated test data is compressed by a data compressor.

Brown et al. does not suggest or disclose a magnetic memory that includes a control system as an integrated component of the magnetic memory where the control system is configured to obtain parametric values from the magnetic memory cells of the magnetic memory and generate corresponding fault maps using the obtained parametric values as recited by claims 1, 2, 25,

and 26. In contrast, Brown et al. teaches the use of a memory tester that is distinct and separate from a memory device under test. More specifically, the memory device to be tested is coupled to the memory tester during the performance of the tests and removed from the memory tester once the tests are complete. Accordingly, Applicants respectfully request that the rejection of claims 1 and claims 2, 25, and 26 be withdrawn.

Amended independent claim 12 and claims 13-14 dependent thereon recite a controller for a magnetic memory which includes at least one array of magnetic memory cells configured to store data. Firmware is configured to store a procedure for obtaining parametric values from magnetic memory cells in the array of magnetic memory cells of a magnetic memory and generate a compressed fault map using the parametric values. A microcontroller is configured to execute the procedure a first time to generate a first compressed fault map. The microcontroller is a component of the magnetic memory and executes the procedure at one or more time intervals after the first time and compares a second compressed fault map generated at each time interval to the first compressed fault map. An indication is provided if there are differences between the second compressed fault map and the first compressed fault map.

Brown et al. does not suggest or disclose the use of a microcontroller that is an integrated component of a magnetic memory and configured to execute a procedure a first time to generate a first compressed fault map, to execute the procedure at one or more time intervals after the first time and to compare a second compressed fault map generated at each time interval to the first compressed fault map as recited by claims 12 and 13-14. Accordingly, Applicants respectfully request that the rejection of claims 12 and 13-14 be withdrawn.

Amended independent claim 19 and claim 20 dependent thereon recite a storage system. The storage system includes *inter alia* at least two magnetic memory storage devices and a control system. The at least two magnetic memory storage devices and control system are components of the storage

system. Each of the at least two magnetic memory storage devices include at least one array of magnetic memory cells configured to store data. The control system is configured to periodically obtain parametric values from magnetic memory cells in the magnetic memory storage devices and generate, using the parametric values, at least one error detection code result. The at least one error detection code result is a compared to a previous at least one error detection code result and an indication is provided if there are differences.

Brown et al. does not suggest or disclose the use of a control system that is an integrated component of a storage system where the control system is configured to periodically obtain parametric values from magnetic memory cells in the magnetic memory storage devices of the storage system and to generate, using the parametric values, at least one error detection code result as recited by claims 19 and 20. Accordingly, Applicants respectfully request that the rejection of claims 19 and 20 be withdrawn.

Amended independent claim 27 and claim 28 dependent thereon recite a method of detecting degradation in at least two magnetic memory cells. Parametric values are periodically obtained from the magnetic memory cells at a magnetic memory, where the magnetic memory cells are components of the magnetic memory. A compressed fault map is generated each time the parametric values are obtained at the magnetic memory. At least one of the compressed fault maps is compared to a previous one of the compressed fault maps at the magnetic memory and an indication is provided if there are differences.

Brown et al. does not suggest or disclose periodically obtaining parametric values from magnetic memory cells of a magnetic memory at the magnetic memory, generating a compressed fault map each time the parametric values are obtained at the magnetic memory, and comparing at least one of the compressed fault maps to a previous one of the compressed fault maps at the magnetic memory as recited by claims 27 and 28. Accordingly, Applicants respectfully request that the rejection of claims 27 and 28 be withdrawn.

Amended independent claim 34 recites a method of detecting degradation in a magnetic memory which includes at least one array of magnetic memory cells configured to store data. The magnetic memory cells are components of a magnetic memory. A procedure for obtaining parametric values from magnetic memory cells in the array of magnetic memory cells is executed and a first compressed fault map is generated from the parametric values at the magnetic memory. For each of at least one time interval, the procedure is executed at the magnetic memory to generate a second compressed fault map. The second compressed fault map is compared to the first compressed fault map at the magnetic memory and an indication is provided if there are differences between the second compressed fault map and the first compressed fault map.

Brown et al. does not suggest or disclose executing a procedure for obtaining parametric values from magnetic memory cells of a magnetic memory at the magnetic memory, generating a first compressed fault map from the parametric values at the magnetic memory, generating a second compressed fault map at the magnetic memory, and comparing the second compressed fault map to the first compressed fault map at the magnetic memory as recited by claim 34. Accordingly, Applicants respectfully request that the rejection of claim 34 be withdrawn.

Claims 3-11, 15-18, 21-24, 29-33, and 35 stand rejected under 35 USC §103(a) as being unpatentable over Brown et al. and in view of Yamada et al. (U.S. Patent No. 6,634,004). Claims 3-11, 25, and 26 depend from independent claim 1 and therefore include the elements recited in independent claim 1. Claims 21-24 depend from independent claim 19 and therefore include the elements recited in independent claim 19. Claims 29-33 depend from independent claim 27 and therefore include the elements recited in independent claim 27. Claim 35 depends from independent claim 34 and therefore includes the elements recited in independent claim 34.

Yamada et al. generally discloses a threshold analysis system for testing memory devices. More specifically, the threshold analysis system determines the threshold voltages of each of the memory cells for each individual memory devices being tested. Applicants respectfully submit that the above-stated deficiencies of the disclosure of Brown et al. with respect to claims 1, 12, 19, 27, and 34 are not cured by the disclosure of Yamada et al. Accordingly, Applicants respectfully request that the rejection of claims 3-11, 15-18, 21-24, 29-33 and 35 as being unpatentable over Brown et al. and in view of Yamada et al. be withdrawn.

Since the prior art does not disclose each of the elements recited by the claims at issue, it follows that such claims are not anticipated thereby.

Furthermore, the prior art does not disclose or suggest that it would be desirable or even possible to obtain parametric values at least twice from the memory cells of a storage device at the storage device and perform a comparison between one set of obtained parametric values with a prior set of obtained parametric values at the storage device as recited by the claims at issue. It is therefore evident that the claims are not obvious thereover. The prior art must disclose at least a suggestion of an incentive for the claimed combination of elements in order for a prima facie case of obviousness to be established. See *In re Sernaker*, 217 U.S.P.Q. 1 (Fed. Cir.1983) and *Ex Parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App.1985). Accordingly, Applicants respectfully request that the rejection of claims 1-35 be withdrawn.

For the foregoing reasons, reconsideration and withdrawal of the rejection of the claims at issue and allowance thereof are respectfully requested.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and change any fees due in connection with this request to Deposit Account no. 08-2025.

Respectfully submitted,

By: Manisha Chakrabarti

Manisha Chakrabarti
Attorney Reg. No. 41,665

Manisha Chakrabarti
Attorney at Law
3108 South Route 59, Suite 124-282
Naperville, Illinois 60564
Telephone: (630) 355-3376

Date: July 3, 2007